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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/127,584	07/31/98	RAYNAUD A	02282.P055

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EXAMINER	
SERGENT, D	
ART UNIT	**PAPER NUMBER**
2763	5

DATE MAILED: 02/01/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/127,584	RAYNAUD ET AL.	
	Examiner	Art Unit	
	Douglas W. Sergent	2763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

14) ☒ Notice of References Cited (PTO-892)
15) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
16) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
17) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
18) ☐ Notice of Informal Patent Application (PTO-152)
19) ☐ Other: .

DETAILED ACTION

1. Claims 1 – 33 have been examined in this application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 24 - 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The application claims identification of a sensitivity list of a process. This sensitivity list (as shown in figure 17) appears to be directed towards identification of signals that are event-sensitive or level-sensitive. It is not clear from the specification if this list is automatically generated, or if this list is generated manually as the code is modified by the insertion of the instrumentation logic.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 14, 16 – 18, 20, 22 – 25 and 28 - 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al ("A Source-Level Dynamic Analysis

Methodology and Tool for High-Level Synthesis", Proceedings of the Tenth International Symposium on System Synthesis, 1997, pp. 134 – 140, September 1997).

With respect to Claim 1 and 5:

Chen et al teaches a methodology and tool for source-level debugging of circuit designs. Specifically, Chen et al teaches:

- Identifying at least one statement in the synthesizable source code (pg. 138, section 4.1, first paragraph).
- Including at least one instrumentation signal indicative of execution status (pg. 137, section 3, daemon is equivalent to claimed instrumentation signal).

With respect to Claim 2:

Chen et al teaches design annotation that includes embedding a daemon in the code describing a circuit element. This daemon is equivalent to the claimed instrumentation logic (pg. 137, sections 3, 3.1; pg. 138, section 3.2).

With respect to Claim 3 and 4:

Chen et al teaches execution analysis that allows for access to variables and operations of the design (pg. 138, section 4.1). The initialization of these variables and the updating of the variables (based on simulation results) is deemed to be inherent in the system of Chen et al.

With respect to Claim 6:

Chen et al teaches design annotation that includes embedding a daemon in the code describing a circuit element. The daemon performs the functions of inserting

unique variable assignment statements for monitoring the output of the current circuit element (pg. 138, figure 3).

With respect to Claim 7:

Chen et al teaches execution analysis that allows for access to variables and operations of the design (pg. 138, section 4.1). The initialization of these variables and the updating of the variables (based on simulation results) is deemed to be inherent in the system of Chen et al.

With respect to Claim 8:

Chen et al teaches creation of instrumentation output signals for the sequential circuit operation (pg. 138, column 1, first paragraph).

With respect to Claim 9:

Chen et al generation cross-reference data mapping for the source code statements and the instrumented output signal (pg. 135, section 2.1).

With respect to Claim 10:

Chen et al teaches simulation of the design using instrumentation signals to establish simulation breakpoints (pg. 138, section 4.1).

With respect to Claim 11:

Chen et al teaches displaying the source code where the code execution is highlighted (pg. 138, section 4.1).

With respect to Claim 12, 16 and 20:

As described previously, Chen et al teaches a method and tools for manipulating a design description using High Level Synthesis (HLS) (as per claimed synthesizable statements). The design annotation process as described in Chen et al section 3 beginning on pg. 137 describes the process of inserting daemons into the source code that allow for the insertion of monitoring variables that can be monitored in the design process. Although Chen et al does not explicitly describe synthesizing the code into a gate-level design, this capability is inherent in the system as the system is used to produce a design description for manufacture.

With respect to Claim 13, 17 and 22:

Chen et al teaches execution analysis that allows for access to variables and operations of the design (pg. 138, section 4.1). The initialization of these variables and the updating of the variables (based on simulation results) is deemed to be inherent in the system of Chen et al.

With respect to Claim 14, 18 and 23:

Chen et al teaches creation of instrumentation output signals for the sequential circuit operation (pg. 138, column 1, first paragraph). Chen et al teaches generation of cross-reference data mapping for the source code statements and the instrumented output (pg. 135, section 2.1).

With respect to Claim 24:

Chen et al teaches the use of a combination of Execution Database and Value Change Database (pg. 137, col. 1 third paragraph; figure 2). These databases collect information from the embedded daemons after simulation has run. However, the iterative design environment would allow for the use of these databases to be reviewed and used as the basis for design changes. In this case, embedded daemons could be placed in the design base on the values in these databases. In this case, the result would be the same as described in claim 24. The design would be reviewed and certain events or values placed in a sensitivity list. This list provides the motivation for insertion of instrumentation logic.

With respect to Claim 25:

Chen et al teaches displaying the source code where the code execution is highlighted (pg. 138, section 4.1).

With respect to Claim 28, 30 and 32:

As described previously, Chen et al teaches a computer-based system (as per claimed storage medium...) to be used for generating a gate-level design from a register transfer level synthesizable source code (pg.137, figure 2). As described previously, the process described by the claimed instrumentation signal are carried out in Chen et al by embedding daemons into the design as part of the design annotation.

With respect to Claim 29:

Chen et al teaches design annotation that includes embedding a daemon in the code describing a circuit element. The daemon performs the functions of inserting unique variable assignment statements for monitoring the output of the current circuit element (pg. 138, figure 3).

With respect to Claim 31 and 33:

Chen et al teaches creation of instrumentation output signals for the sequential circuit operation (pg. 138, column 1, first paragraph). Chen et al teaches generation of cross-reference data mapping for the source code statements and the instrumented output (pg. 135, section 2.1).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 15, 19, 21, 26 and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al as applied to claims 12, 16, 20 and 24 above, in view of Koch et al.("Debugging of Beharioral VHDL Specifications by Source Level Emulation", Proceedings of the European Design Automation Conference, pp. 256 - 261, September 1995).

With respect to Claim 15, 19 and 21:

Chen et al teaches the ability to give the user to access individual statements for "setting stop points and the access to variables and operations for displaying values" (pg. 138, section 4.1). Chen et al does not explicitly describe the stop points as being activated by transition of the breakpoint signal to a pre-determined value.

Koch et al teaches VHDL specification debugging with the use of an emulator. Koch et al describes modification of the source code to include insertion of registers to provide the ability to read out values (pg. 258, section 3, first paragraph). This allows for the establishment of breakpoints based on the output of a comparator gate, indicating that a required value has been reached (pg. 258, section 3, second paragraph). It would have been obvious to one skilled in the art at the time of the applicant's invention to include the ability to set breakpoints based on specific outputs in order to debug both signal events and signal levels where appropriate.

With respect to Claim 26 and 27:

Chen et al teaches generation of instrument signals based on the insertion of embedded daemons. Chen et al does not explicitly address sampling particular signals or comparing these signals to the corresponding instrument signal, or of generating a signal based on logically ORing these signals.

Koch et al teaches the use of state and condition comparators (pg. 259, first paragraph; figure 3). These comparators allow for the comparison of values for setting breakpoints.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Kucukcakar et al describes the Matisse system (the system used in Chen et al).
- Fang et al describes a method for making real time changes to an RTL design using on-line debugging.
- Stapleton teaches an object oriented system for simulation that supports debugging of the source code (not standard HDL however.)
- Dangelo et al teaches a system for debugging VHDL designs.
- Ault et al teaches a software debugging system.
- Carbine teaches a apparatus for debugging a VLSI chip

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Sergent whose telephone number is (703)306-5448. The examiner can normally be reached on M-F (6:30 - 4:00) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703)305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-1396 for regular communications and (703)308-1396 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-5140.

Doug Sergent/DS
January 27, 2000

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER